

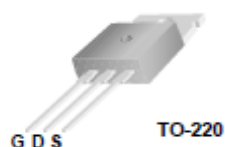


TSP50N20M

200V N-Channel MOSFET

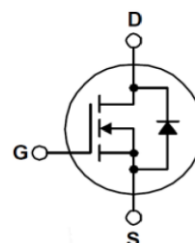
General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.



Features

- 50A, 200V, Max. $R_{DS(on)} = 0.051\Omega$ @ $V_{GS} = 10V$
- Low gate charge: $Q_g = 80nC$ (Typ.)
- Low drain-source On resistance: $R_{DS(on)} = 51m\Omega$ (Max.)
- 100% avalanche tested
- RoHS compliant device



Absolute Maximum Ratings $T_c = 25^\circ C$ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		200	V
V_{GS}	Gate-Source Voltage		± 30	V
I_D	Drain Current	$T_c = 25^\circ C$	50	A
		$T_c = 100^\circ C$	31.6	A
I_{DM}	Pulsed Drain Current		200	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1333	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	19.8	mJ
I_{AR}	Repetitive Avalanche current	(Note 1)	50	A
P_D	Power Dissipation ($T_c = 25^\circ C$)		175	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.71	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ C/W$

Electrical Characteristics $T_c=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$	--	0.043	0.051	Ω
R_g	Internal gate resistance	Open drain, $f=1\text{ MHz}$	--	1	--	Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	200	--	--	V
I_{DSS}	Drain-source cut-off current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 160\text{ V}, T_c = 125\text{ }^{\circ}\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	3800	--	pF
C_{oss}	Output Capacitance		--	480	--	pF
C_{rss}	Reverse Transfer Capacitance		--	64	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 100\text{ V}, I_D = 50\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4)	--	57	--	ns
t_r	Turn-On Rise Time		--	28	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	169	--	ns
t_f	Turn-Off Fall Time		--	44	--	ns
Q_g	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 50\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 3,4)	--	80	--	nC
Q_{gs}	Gate-Source Charge		--	18.5	--	nC
Q_{gd}	Gate-Drain Charge		--	25.5	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I _S	Continuous Source-Drain Diode Forward Current		--	--	50	A
I _{SM}	Pulsed Source-Drain Diode Forward Current		--	--	200	
V _{SD}	Source-Drain Diode Forward Voltage	I _S =50A, V _{GS} = 0 V	--	--	1.5	V
t _{rr}	Reverse Recovery Time	I _S =50, V _{GS} = 0 V di _F /dt = -100 A/μs (Note 3, 4)	--	282	--	ns
Q _{rr}	Reverse Recovery Charge		--	2.3	--	uC

NOTES:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=0.8\text{ mH}, I_{AS}=50\text{ A}, V_{DD}=50\text{ V}, R_G=25\text{ }\Omega$, Starting $T_J=25\text{ }^{\circ}\text{C}$
3. Pulse test: Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Fig. 1 $I_D - V_{DS}$

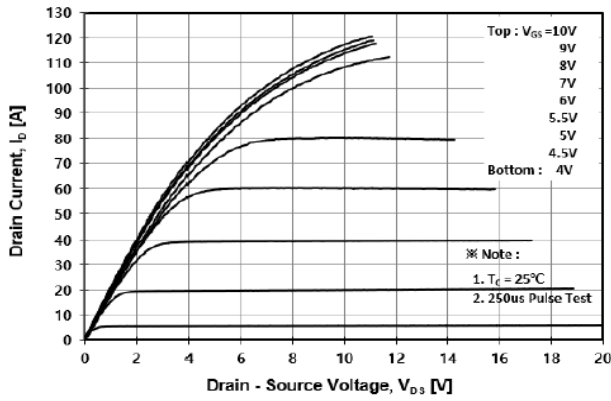


Fig. 2 $I_D - V_{GS}$

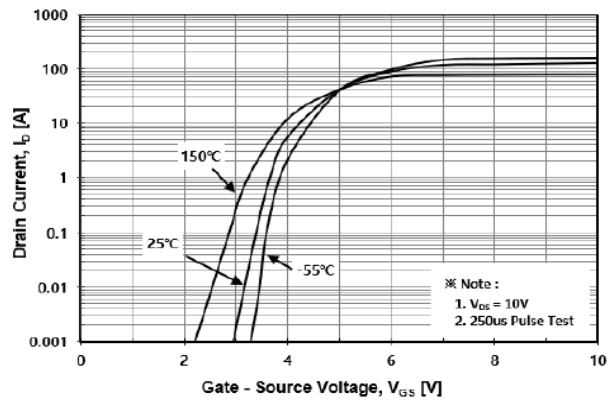


Fig. 3 $R_{DS(ON)} - I_D$

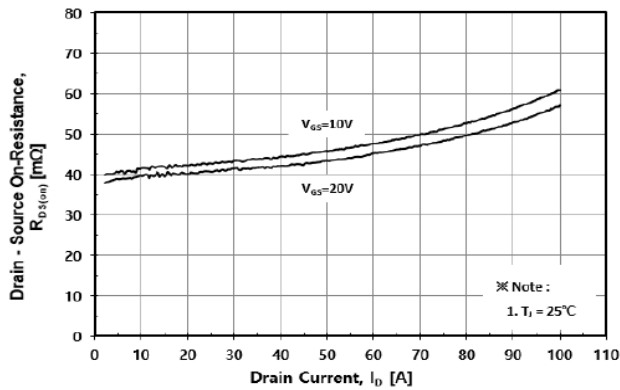


Fig. 4 $I_S - V_{SD}$

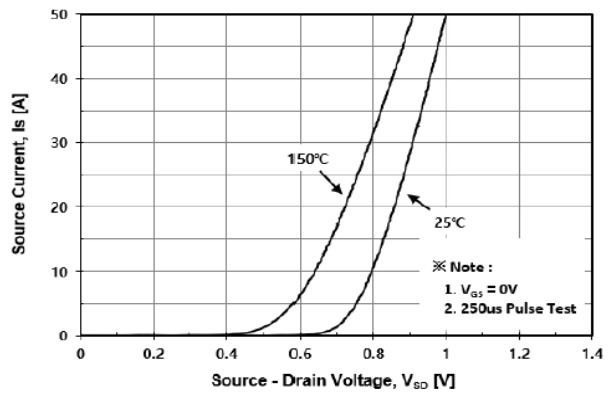


Fig. 5 Capacitance - V_{DS}

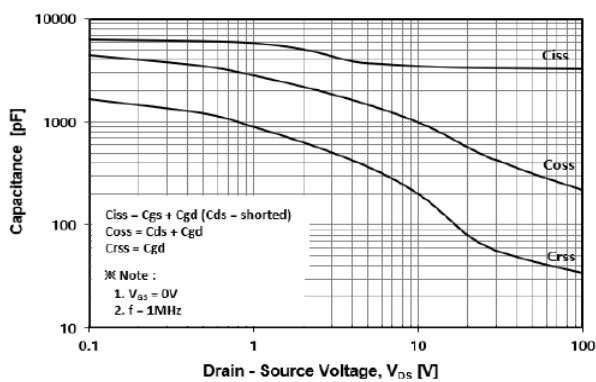
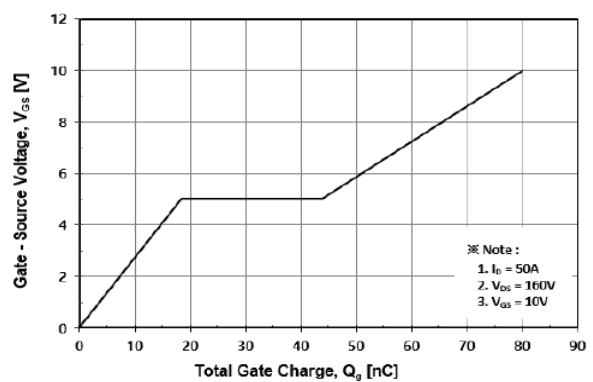


Fig. 6 $V_{GS} - Q_G$



Typical Characteristics Curve (Continue)

Fig. 7 $BV_{DSS} - T_J$

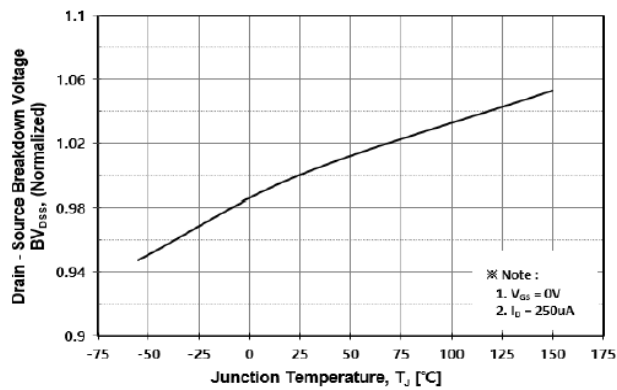


Fig. 8 $R_{DS(ON)} - T_J$

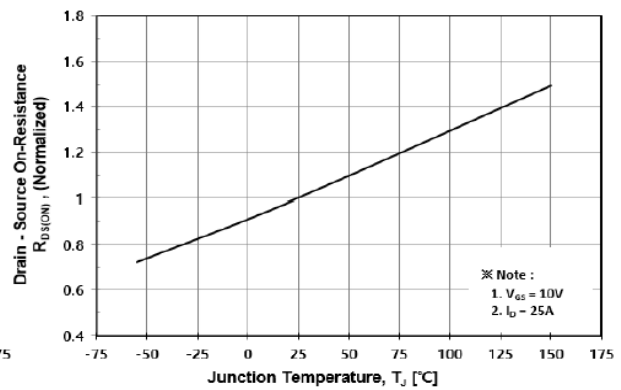


Fig. 9 $I_D - T_C$

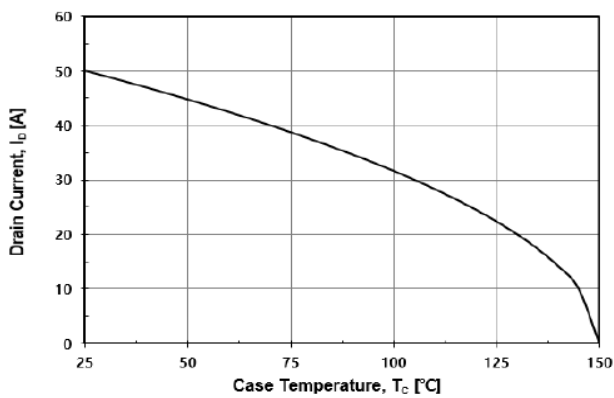


Fig. 10 Safe Operating Area

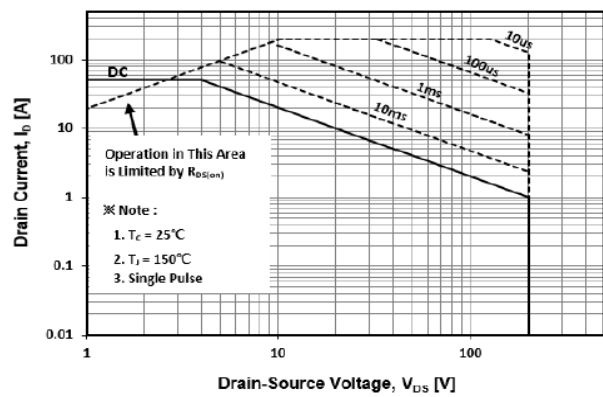


Fig. 11 Transient Thermal Impedance

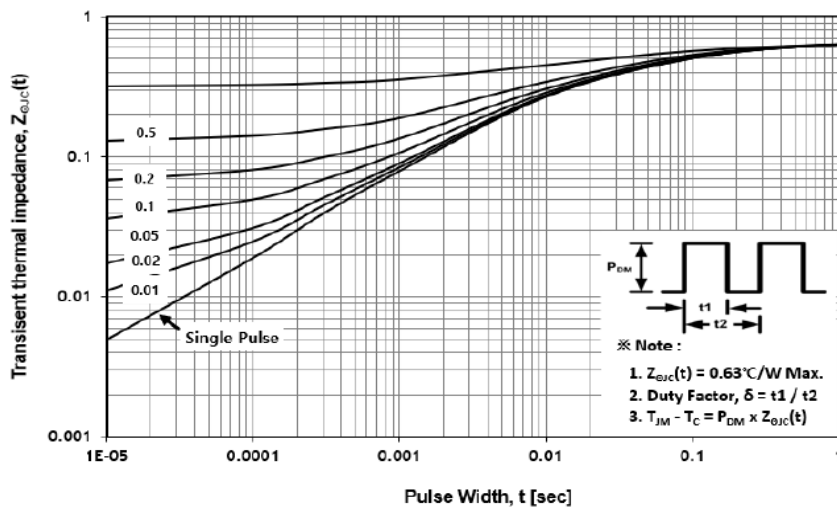


Fig. 12 Gate Charge Test Circuit & Waveform

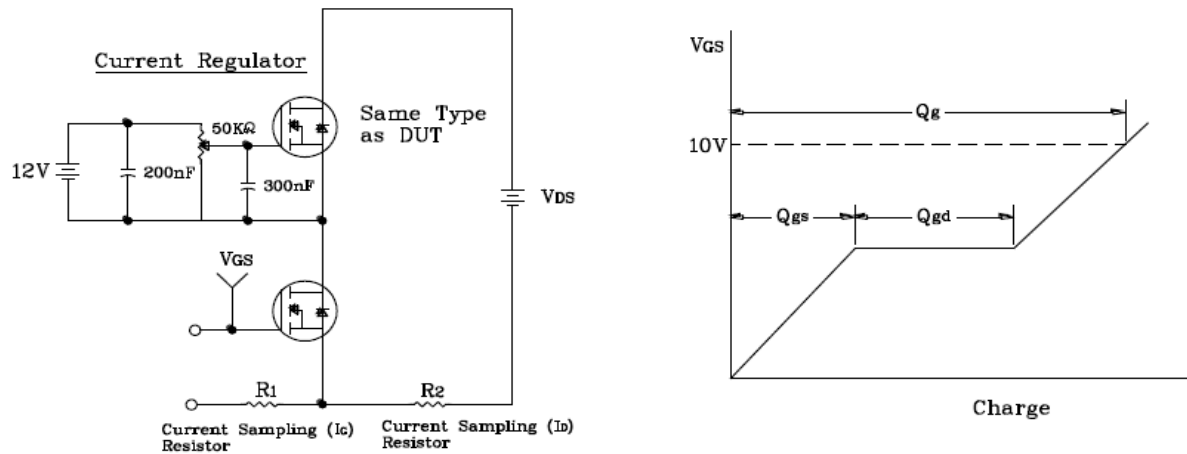


Fig. 13 Resistive Switching Test Circuit & Waveform

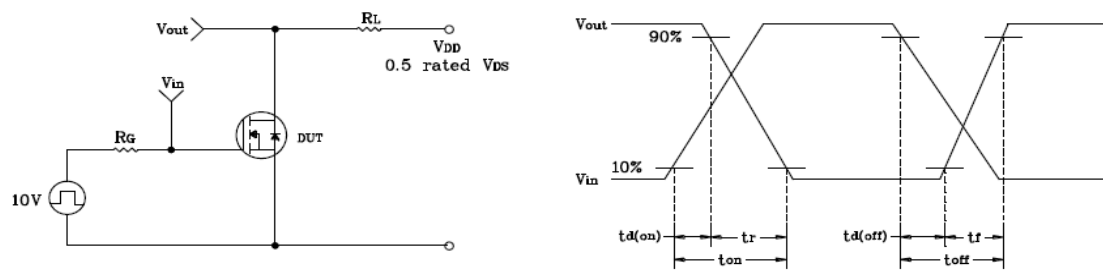


Fig. 14 E_{AS} Test Circuit & Waveform

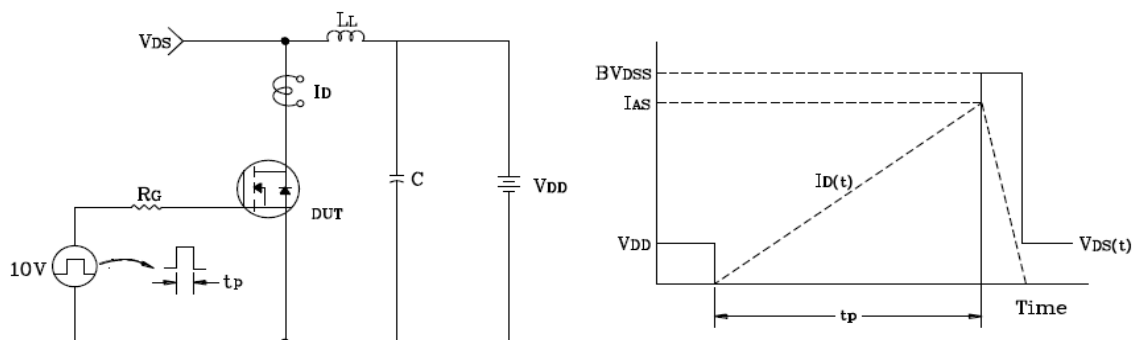


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

