



TSP18N20M

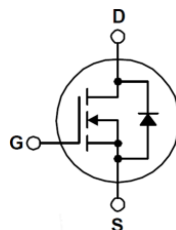
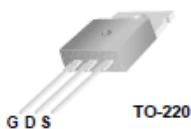
200V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 18A,200V,Max. $R_{DS(on)}$ =0.17 Ω @ V_{GS} =10V
- Low gate charge(typical 22nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

$T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		200	V
V_{GS}	Gate-Source Voltage		± 30	V
I_D	Drain Current	$T_C = 25^{\circ}\text{C}$	18*	A
		$T_C = 100^{\circ}\text{C}$	9.1*	A
I_{DM}	Pulsed Drain Current		72*	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	453	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	13.9	mJ
I_{AR}	Repetitive avalanche current	(Note 1)	18	A
P_D	Power Dissipation ($T_C = 25^{\circ}\text{C}$)		100	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^{\circ}\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Resistance Characteristics

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	1.5	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	62.5	$^{\circ}\text{C/W}$

Electrical Characteristics $T_C=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$	--	0.14	0.17	Ω
g_{fs}	Forward transfer conductance(note 3)	$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$	--	35	--	S

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	200	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current,Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current,Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	965	--	pF
C_{oss}	Output Capacitance		--	227	310	pF
C_{rss}	Reverse Transfer Capacitance		--	55	71	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 125\text{ V}, I_D = 18\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 3,4)	--	15	--	ns
t_r	Turn-On Rise Time		--	130	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	135	--	ns
t_f	Turn-Off Fall Time		--	105	--	ns
Q_g	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 3,4)	--	22	28	nC
Q_{gs}	Gate-Source Charge		--	6.6	--	nC
Q_{gd}	Gate-Drain Charge		--	7.2	--	nC

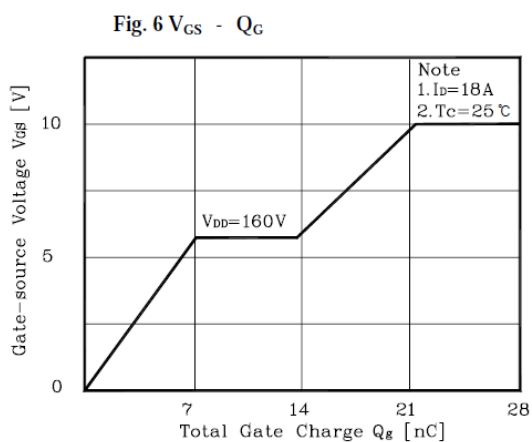
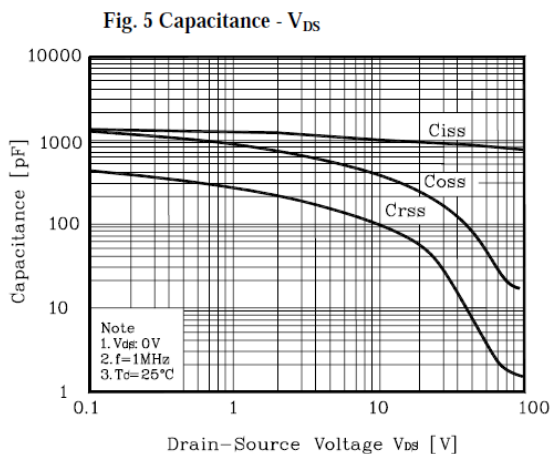
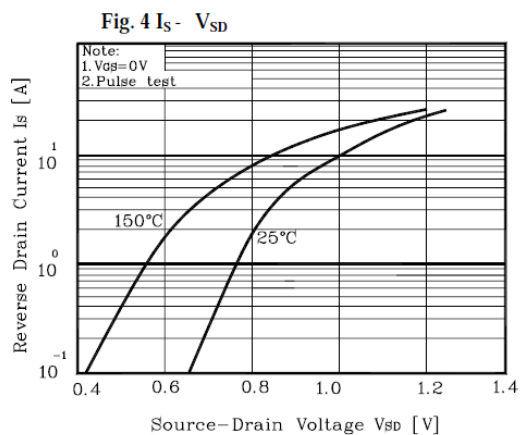
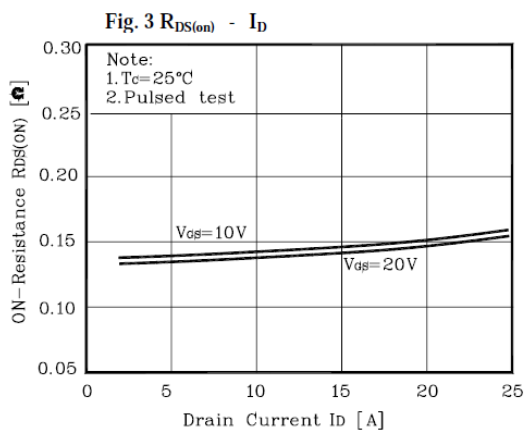
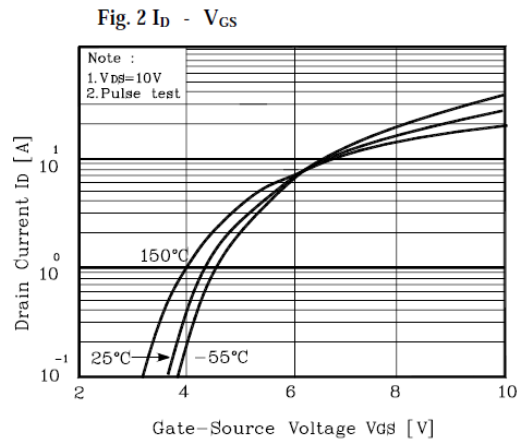
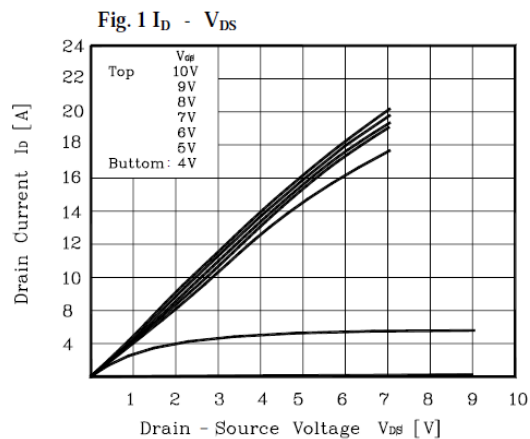
Source-Drain Diode Maximum Ratings and Characteristics

I _S	Continuous Source-Drain Diode Forward Current		--	--	18	A
I _{SM}	Pulsed Source-Drain Diode Forward Current (Note 1)		--	--	72	
V _{SD}	Source-Drain Diode Forward Voltage	I _S = 18A, V _{GS} = 0 V	--	--	1.4	V
t _{rr}	Reverse Recovery Time	I _S = 18A, V _{GS} = 0 V di _F /dt = 100 A/μs (Note 4)	--	208	--	ns
Q _{rr}	Reverse Recovery Charge		--	1.63	--	μC

Note:

1. Repeated rating: Pulse width limited by maximum junction temperature
2. $L=2.1\text{ mH}$, $I_{AS}=18\text{ A}$, $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, Starting $T_J=25\text{ }^{\circ}\text{C}$
3. Pulse test: Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature

Typical Characteristics



Typical Characteristics

Fig. 7 $V_{DS} - T_J$

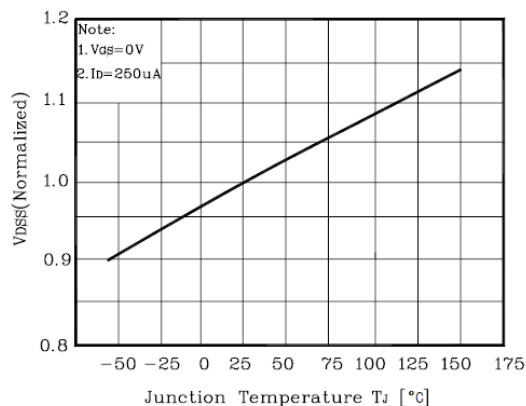


Fig. 8 $R_{DS(on)} - T_J$

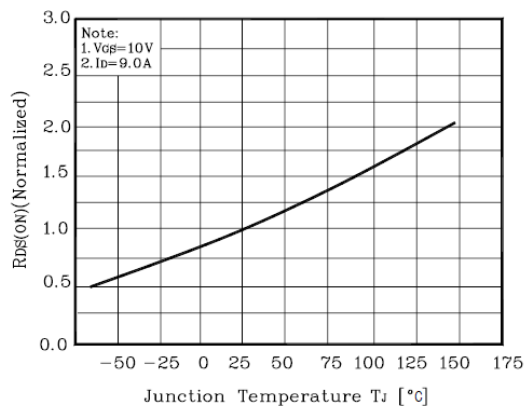


Fig. 9 $I_D - T_C$

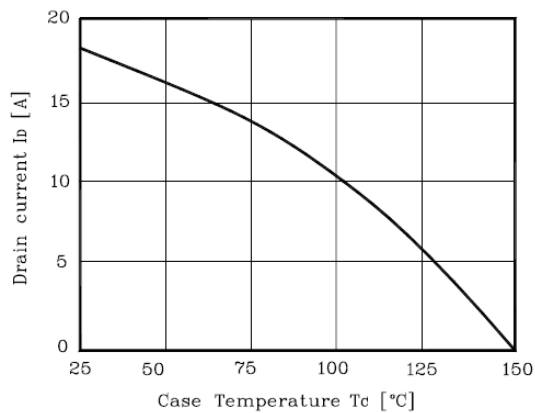


Fig. 10 Safe Operating Area

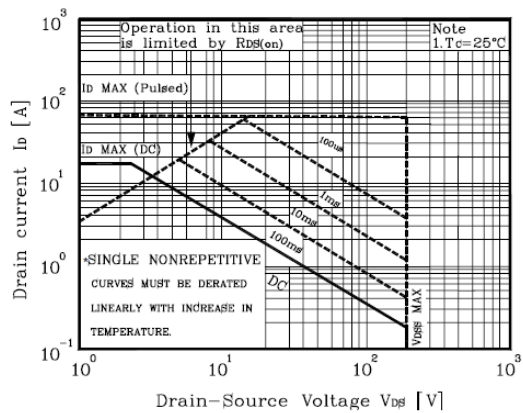


Fig 11. Gate Charge Test Circuit & Waveform

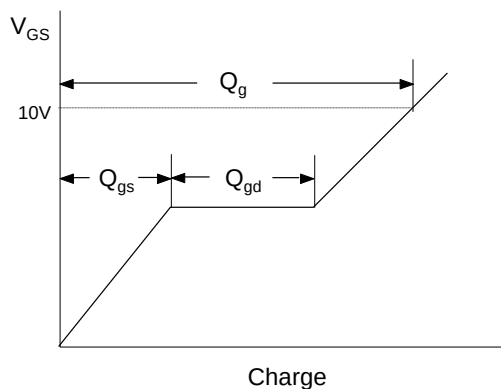
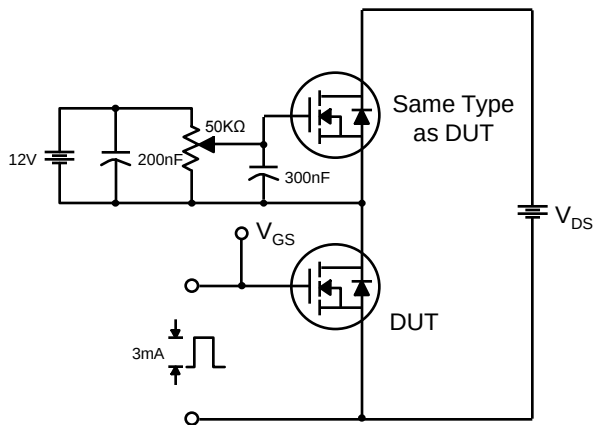


Fig 12. Resistive Switching Test Circuit & Waveforms

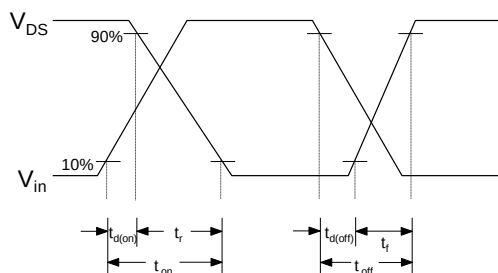
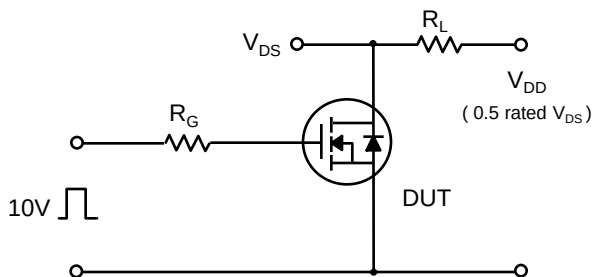


Fig 13. Unclamped Inductive Switching Test Circuit & Waveforms

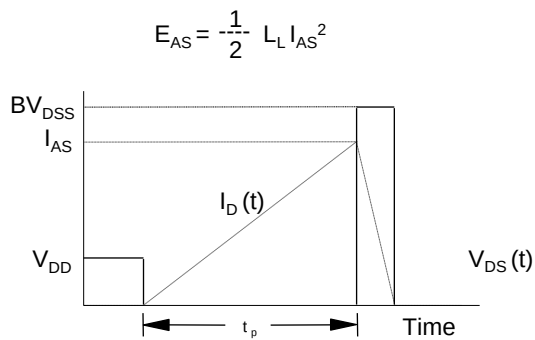
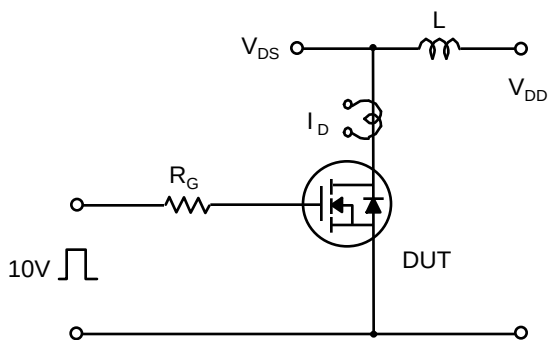


Fig 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

