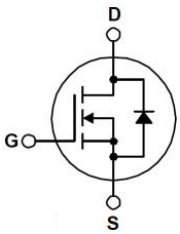
TSF4N90M
900V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- Drain-Source breakdown voltage: BVDSS=900V (Min.)
- Low gate charge: Qg=22nC (Typ.)
- Low drain-source On resistance: RDS(on)=4.2Ω (Max.)
- 100% avalanche tested
- RoHS compliant device



Absolute maximum ratings (T_C=25°C unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V_{DSS}		900	V
Gate-source voltage	V_{GSS}		±30	V
Drain current (DC) *	I_D	T_c=25°C	4	A
		T_c=100°C	2.53	A
Drain current (Pulsed) *	I_{DM}		16	A
Single avalanche current (Note 2)	I_{AS}		4	A
Single pulsed avalanche energy (Note 2)	E_{AS}		84.7	mJ
Repetitive avalanche current (Note 1)	I_{AR}		4	A
Repetitive avalanche energy (Note 1)	E_{AR}		4	mJ
Power dissipation	P_D		40	W
Junction temperature	T_J		150	°C
Storage temperature range	T_{stg}		-55~150	°C

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 3.13	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	I_D=250uA, V_{GS}=0V	900	-	-	V
Gate threshold voltage	$V_{GS(th)}$	I_D=250uA, V_{DS}=V_{GS}	3	4	5	V
Drain-source cut-off current	I_{DSS}	V_{DS}=900V, V_{GS}=0V	-	-	1	uA
Gate leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=2A	-	3.7	4.2	Ω
Forward transfer conductance (Note 3)	g_{fs}	V_{DS}=10V, I_D=2A	-	4	-	S
Input capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	750	-	pF
Output capacitance	C_{oss}		-	62	-	
Reverse transfer capacitance	C_{rss}		-	12	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	V_{DD}=450V, I_D=4A, R_G=25Ω	-	38	-	ns
Rise time (Note 3,4)	t_r		-	60	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	68	-	
Fall time (Note 3,4)	t_f		-	54	-	
Total gate charge (Note 3,4)	Q_g	V_{DS}=720V, V_{GS}=10V, I_D=4A	-	22	-	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	8	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	7	-	

Source-Drain Diode Ratings and Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	4	A
Source current (Pulsed)	I_{SM}		-	-	16	A
Forward voltage	V_{SD}	V_{GS}=0V, I_S=4A	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	I_S=4A, V_{GS}=0V dI_F/dt=100A/us	-	301	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	2.06	-	uC

Note:
1. Repeated rating: Pulse width limited by safe operating area
2. L=10mH, I_{AS}=4A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. Pulse test: Pulse width≤300us, Duty cycle≤2%
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

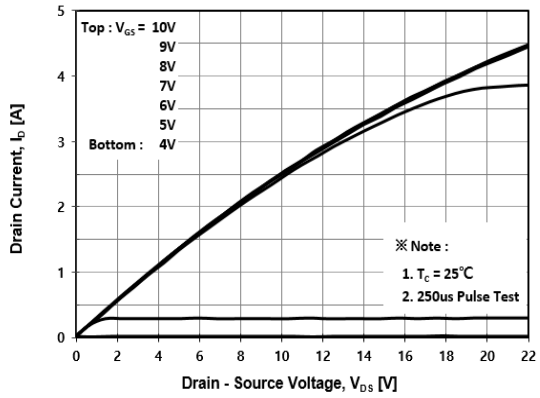


Fig. 2 Typical Transfer Characteristics

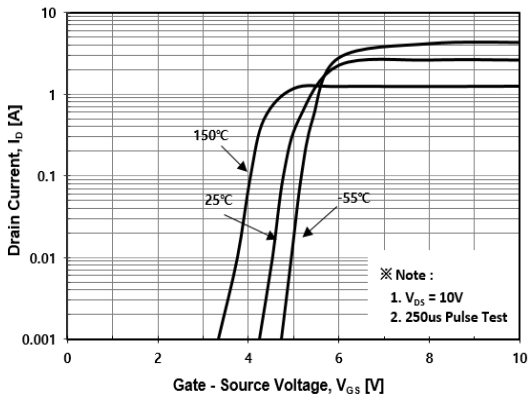


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

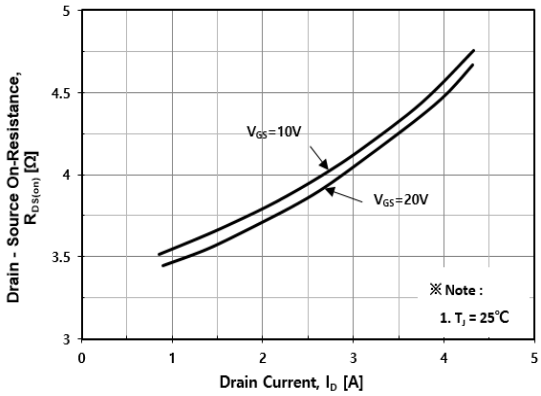


Fig. 4 Body Diode Forward Voltage Variation with Source Current

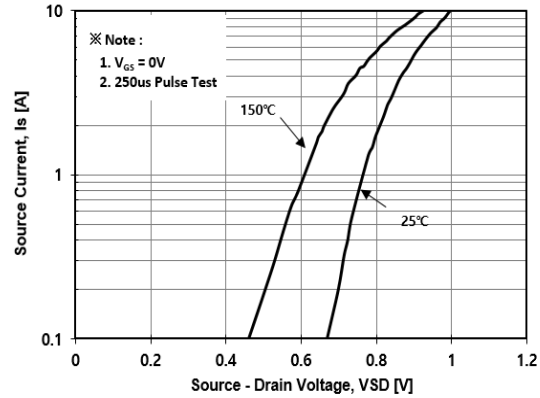


Fig. 5 Typical Capacitance Characteristics

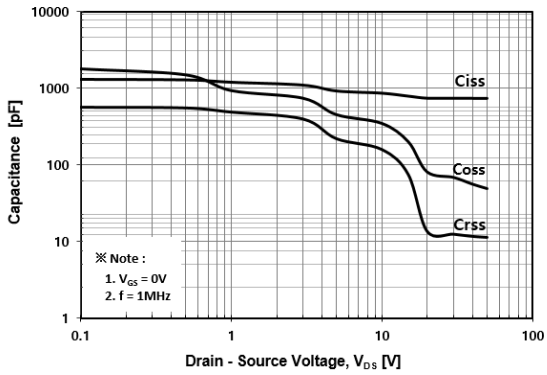
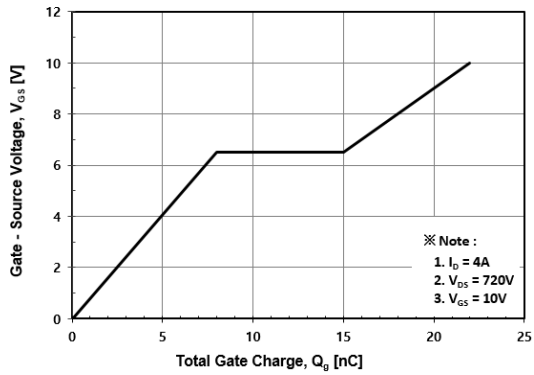


Fig. 6 Typical Total Gate Charge Characteristics



Electrical Characteristics Curves

Fig. 7 Breakdown Voltage Variation vs. Temperature

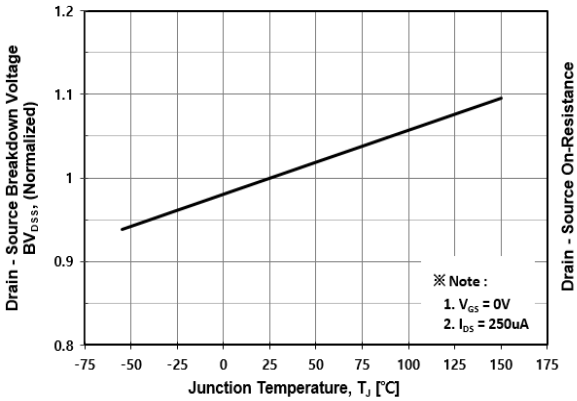


Fig. 8 On-Resistance Variation vs. Temperature

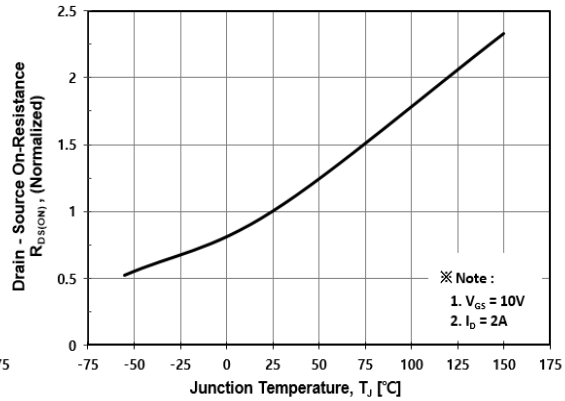


Fig. 9 Maximum Drain Current vs. Case Temperature

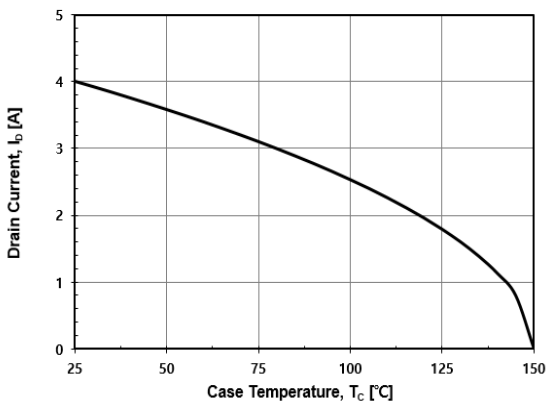


Fig. 10 Maximum Safe Operating Area

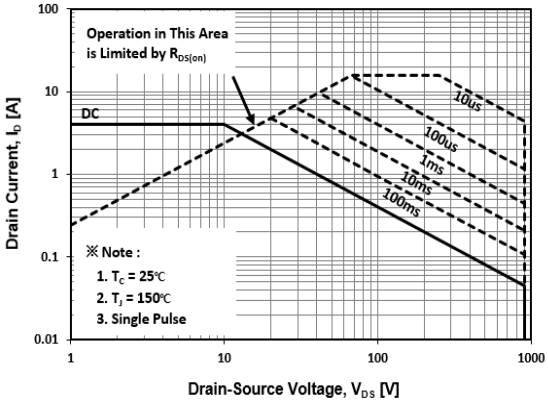


Fig. 11 Transient Thermal Impedance

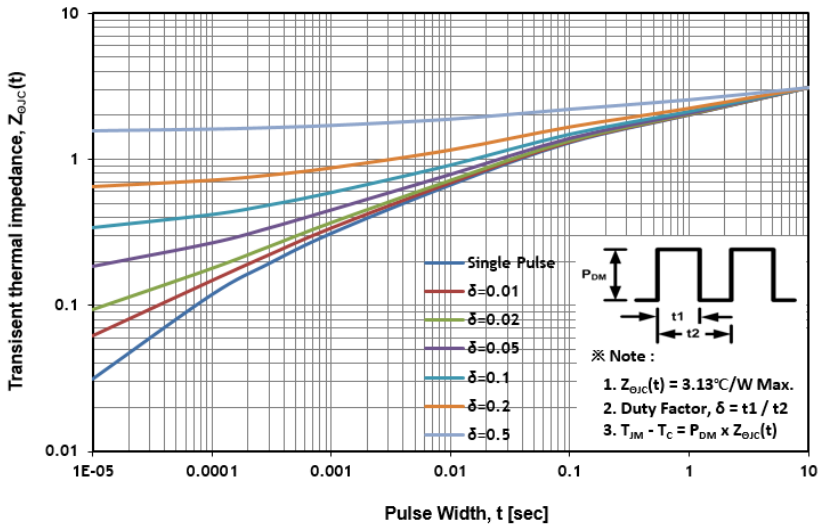
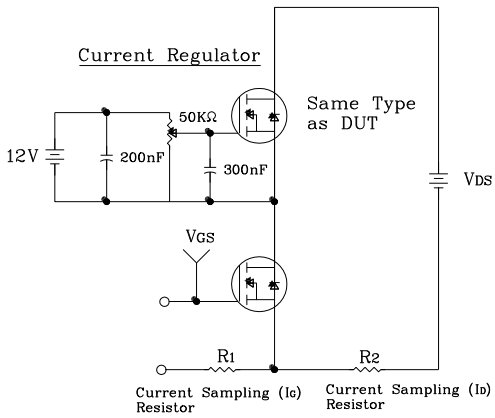


Fig. 12 Gate Charge Test Circuit & Waveform



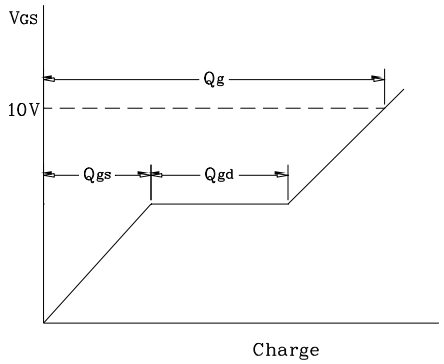
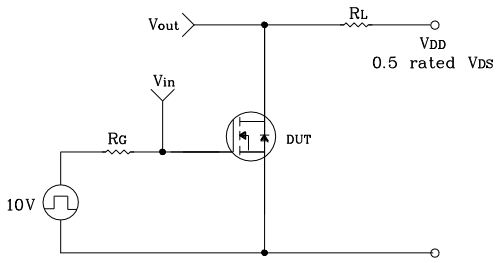


Fig. 13 Resistive Switching Test Circuit & Waveform



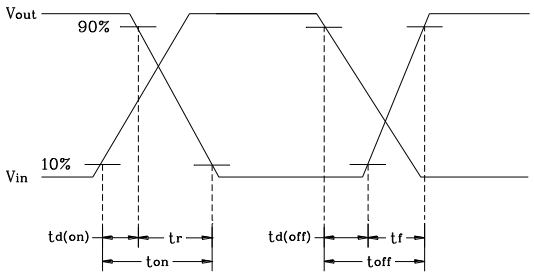
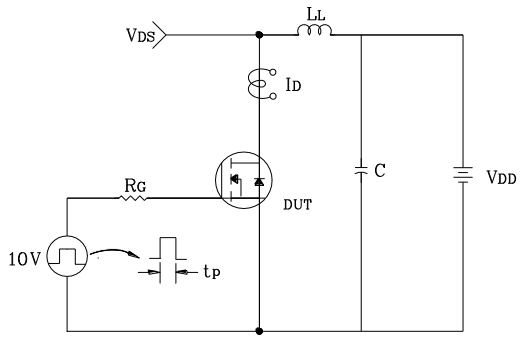


Fig. 14 E_{AS} Test Circuit & Waveform



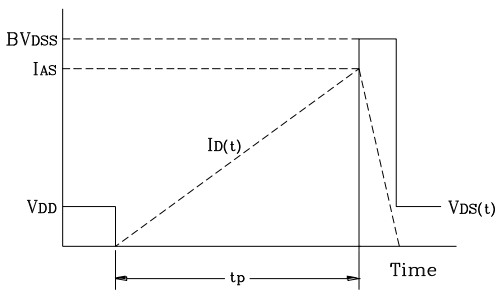


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform